

## Description

The UC3842B/43B series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

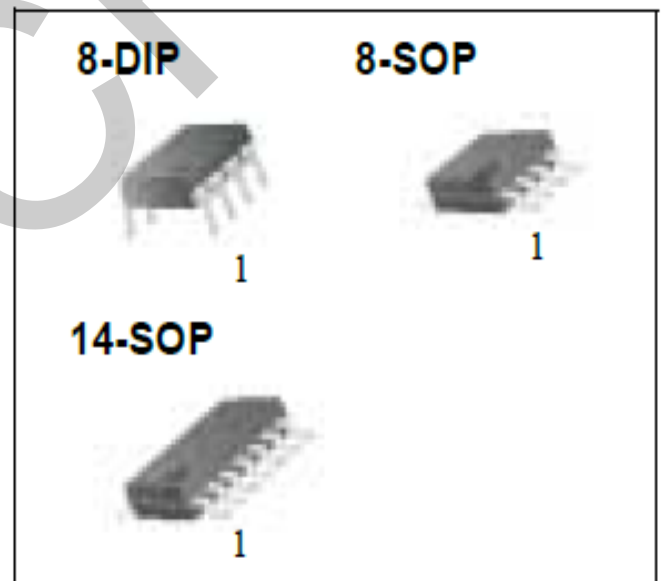
Also included are protective features consisting of input and reference under voltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output dead time, and a latch for single pulse metering.

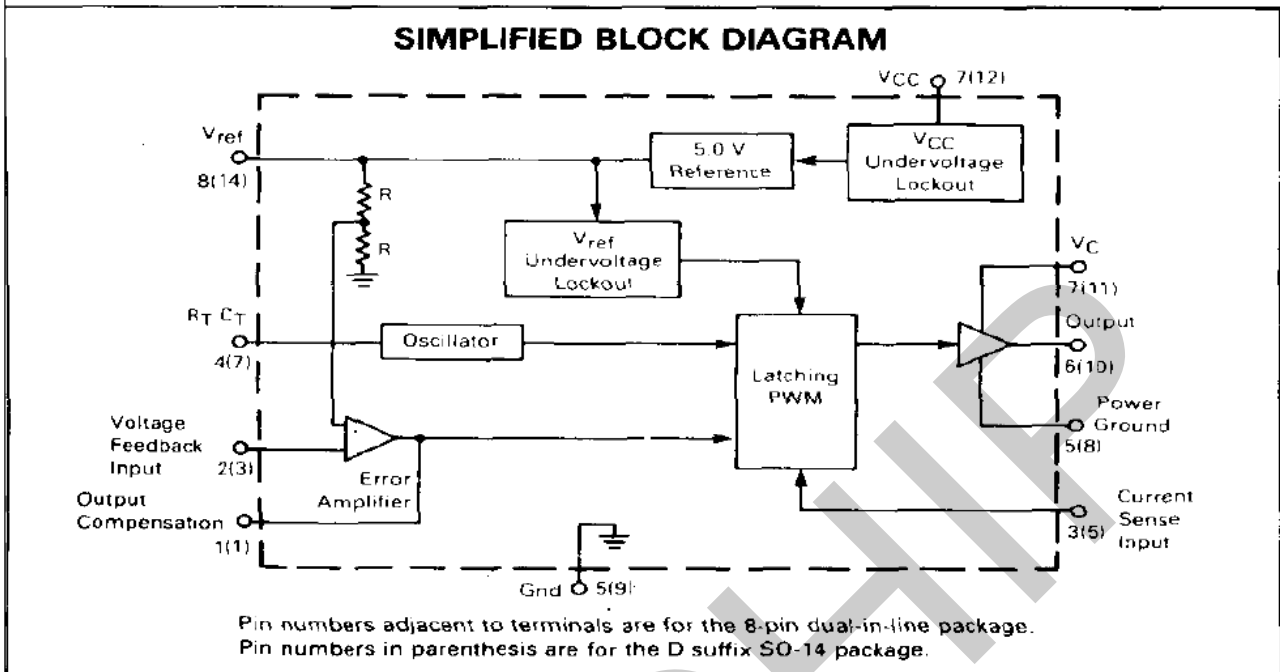
These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 8-pin plastic surface mount (SO-8). And 14-pin plastic surface mount (SO-14). SO-14 package Figure Teng column output stage has a separate power and ground pins.

Difference between members of this series is the under-voltage lockout thresholds. The UC3842B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The corresponding thresholds for the UC3843B are 8.5 V and 7.9 V.

## Feature

- ◆ Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- ◆ Current Mode Operation to 500 kHz
- ◆ Automatic Feed Forward Compensation
- ◆ Latching PWM for Cycle-By-Cycle Current Limiting
- ◆ Internally Trimmed Reference with Under voltage Lockout
- ◆ High Current Totem Pole Output
- ◆ Under voltage Lockout with hysteresis
- ◆ Low Start-Up and Operating Current





### Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Total Power Supply and Zenger Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	$I_O$	1	A
Output Energy (Capacitive Load per Cycle)	$w$	5	uJ
Current Sense and Voltage Feedback Inputs	$V_{in}$	-0.3 to +5.5	V
Error Amp Output Sink Current	$I_O$	10	mA
Power Dissipation and Thermal Characteristics			
NF Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	862	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	$^\circ\text{C/W}$
N Suffix, Plastic Package			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.25	W
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Operating Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Operating Ambient Temperature	$T_A$	0 to +70	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

**Electrical Characteristics** ( $V_{CC}=15\text{ V}$  [Note 2],  $R_T=10\text{ k}$ ,  $C_T=3.3\text{ nF}$ ,  $T_A=T_{LOW}$  to  $T_{HIGH}$  [Note 3] unless otherwise noted)

Characteristic	UC3842B/43B				
	Symbol	Min	Typ	Max	Unit
Reference Section					
Reference Output Voltage ( $I_o=1.0\text{ mA}$ , $T_J=25^\circ\text{C}$ )	$V_{ref}$	4.9	5.0	5.1	V
Line Regulation ( $V_{CC}=12\text{ V}$ to $25\text{ V}$ )	$Reg_{line}$	—	2.0	20	mV
Load Regulation ( $I_o=1\text{ mA}$ to $20\text{ mA}$ )	$Reg_{load}$	—	3.0	25	mV
Temperature Stability	$T_S$	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	$V_{ref}$	4.82	—	5.18	V
Temperature Output Noise Voltage ( $f=10\text{ Hz}$ to $10\text{ kHz}$ ,	$V_n$	—	50	—	$\mu\text{V}$
$T=25^\circ\text{C}$ ) Long Term Stability ( $T_A=125^\circ\text{C}$ for 1000 Hours)	S	—	5.0	—	mV
Output Short Circuit Current	$I_{sc}$	-30	-85	-180	mA
Oscillator Section					
Oscillation Frequency					
$T_J=25^\circ\text{C}$	$f_{osc}$	47	52	57	kHz
$T_A=T_{LOW}$ to $T_{HIGH}$		46	—	60	
Frequency Change with Voltage ( $V_{CC}=12\text{ V}$ to $25\text{ V}$ )	$\Delta f_{osc}/\Delta V$	—	0.2	1	%
Frequency Change with Temperature $T_A=T_{LOW}$ to $T_{HIGH}$	$\Delta f_{osc}/\Delta V$	—	0.5	—	%
Oscillator Voltage Swing (Peak-to-Peak)	$V_{osc}$	—	1.6	—	V
Discharge Current ( $V_{osc}=2.0\text{ V}$ )					
$T_J=25^\circ\text{C}$	$I_{dischg}$	7.5	8.4	9.3	mA
$T_A=T_{LOW}$ to $T_{HIGH}$		7.2	—	9.5	

Notes: 1. Maximum Package power dissipation limits must be observed.

2. Adjust  $V_{CC}$  above the Start-Up threshold before setting to  $15\text{ V}$ .

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.  $T_{LOW} = 0^\circ\text{C}$   $T_{HIGH} = +70^\circ\text{C}$

4. This parameter is measured at the latch trip point with  $V_{FB} = 0\text{ V}$

$$A_v = \frac{\Delta V_{OUTPUT/COMP}}{\Delta V_{CURRENTSENSE}}$$

5. Comparator gain is defined as:

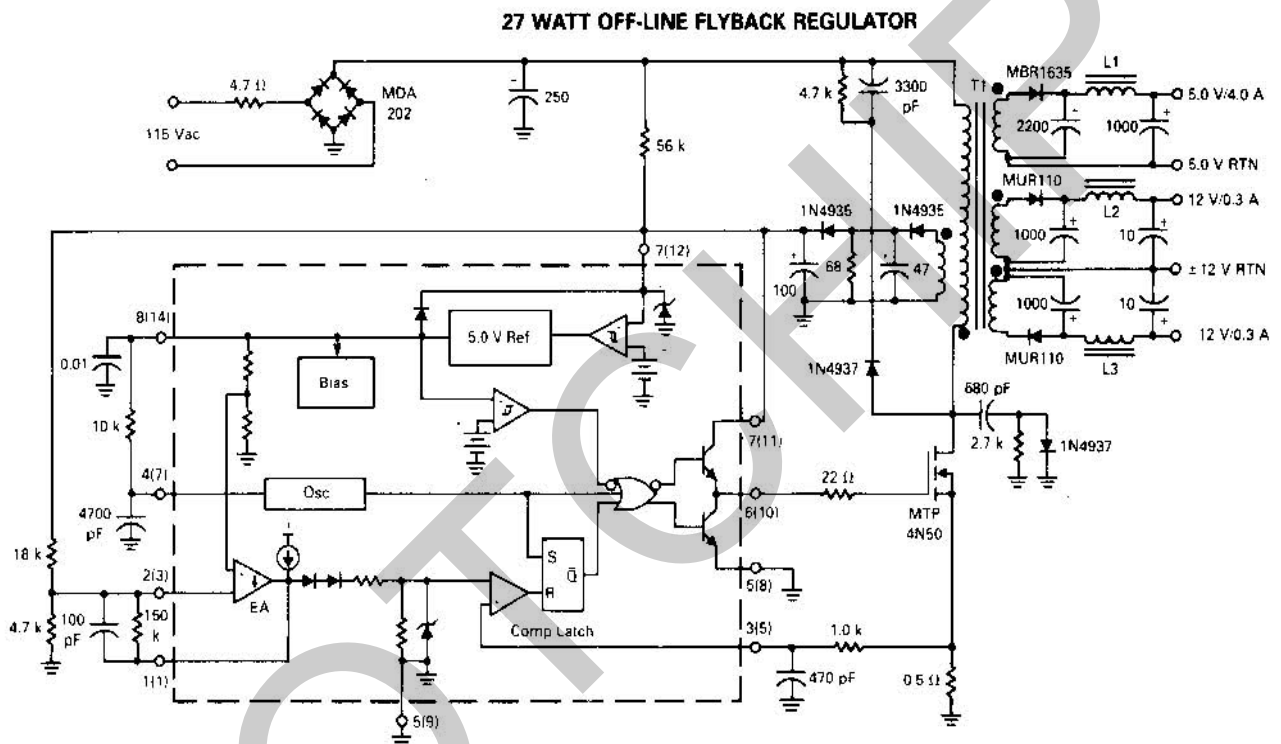
### Electrical Characteristics (V<sub>CC</sub>=15 V [Note 2], R<sub>T</sub>=10 k, C<sub>T</sub>=3.3 nF, T<sub>A</sub>=T<sub>LOW</sub> to T<sub>HIGH</sub> [Note 3]

unless otherwise noted)

Characteristic	UC3842B/43B					
	Symbol	Min	TYP	Max	Unit	
<b>Error Amplifier Section</b>						
Voltage Feedback Input (V <sub>0</sub> =2.5 V)	V <sub>FB</sub>	2.42	2.5	2.58	V	
Input Bias Current (V <sub>FB</sub> =5.0V)	I <sub>IB</sub>	—	-0.1	-2	μA	
Open-Loop Voltage Gain (V <sub>0</sub> =2.0 V to 4.0 V)	A <sub>VOL</sub>	65	90	—	dB	
Unity Gain Bandwidth (T <sub>J</sub> =25°C)	BW	0.7	1	—	MHz	
Power Supply Rejection Ratio (V <sub>CC</sub> =12 V to 25 V)	PSRR	60	70	—	dB	
V	I <sub>Sink</sub>	2	12	—	mA	
	I <sub>Source</sub>	-0.5	-1	—		
Output Voltage Swing	V <sub>OH</sub> V <sub>OL</sub>	5 —	6.2 0.8	— 1.1	V	
High State (R <sub>L</sub> =15 k to ground, V <sub>FB</sub> =2.3 V)						
Low State (R <sub>L</sub> =15 k to V <sub>ref</sub> , V <sub>FB</sub> =2.7 V)						
<b>Current Sense Section</b>						
Current Sense Input Voltage Gain (Notes 4 & 5)	A <sub>v</sub>	2.85	3	3.15	V/V	
Maximum Current Sense Input Threshold (Note 4)	V <sub>th</sub>	0.9	1	1.1	V	
Power Supply Rejection Ratio (V <sub>CC</sub> =12 V to 25V, Note 4)	PSRR	—	70	—	dB	
Input Bias Current	I <sub>IB</sub>	—	-2	-10	μA	
Propagation Delay (Current Sense Input to Output)	t <sub>PLH(IN/OUT)</sub>	—	150	300	ns	
<b>Output Section</b>						
Output Voltage	V <sub>OL</sub> V <sub>OH</sub>	— 13	0.1 13.5	0.4 —	V	
Low State (I <sub>Sink</sub> =20 mA) (I <sub>Sink</sub> =200 mA)						
High State (I <sub>Source</sub> =20 mA) (I <sub>Source</sub> =200 mA)		12	13.4	—		
Output Voltage with UVLO Activated V <sub>CC</sub> =6.0 V, I <sub>Sink</sub> =1.0 mA	V <sub>OL(UVLO)</sub>	—	0.1	1.1	V	
Output Voltage Rise Time (C <sub>L</sub> =1.0 nF, T <sub>J</sub> =25°C)	t <sub>r</sub>	—	50	150	ns	
Output Voltage Fall Time (C <sub>L</sub> =1.0 nF, T <sub>J</sub> =25°C)	t <sub>f</sub>	—	50	150	ns	
<b>Under Voltage Lockout Section</b>						
Start-Up Threshold (UC3842B/43B)	V <sub>th</sub>	14.5/7.8	16/8.4	17.5/9.0	V	
Minimum Operating Voltage After Turn-On UC3842B UC3843B	V <sub>CC(min)</sub>	8.5	10	11.5		
		7.0	7.6	8.2		
<b>PWM Section</b>						
Duty Cycle	Maximum	D <sub>max</sub>	94	96	—	%
	Minimum	D <sub>min</sub>	—	—	0	
<b>Total Device</b>						

Power Supply Current Start-Up ( $V_{CC}=14\text{ V}$ for UC3842B $V_{CC}=6.5\text{ V}$ for UC3843B )	$I_{CC}+I_C$	—	0.15	0.3	mA
Power Operating Supply Current (Note 2)	$I_{CC}+I_C$	—	12	17	mA
Power Supply Zener Voltage ( $I_{CC}=25\text{ mA}$ )	$V_Z$	30	36	—	V

### TYPICAL APPLICATION



T1-Primary :45 Turns#26 AWGL1-15 $\mu$ h at 5.0A, Coil craft Z7256

Secondary  $\pm 12\text{V}$ :9 Turns #30 AWG (2 strands) Bifilar Wound L2,L3-25 $\mu$ h at 1.0A, Coil craft

Z7257Secondary 5.0V:4 Turns (six strands)#26 Hexfiliar Wound

Secondary Feedback:10 Turns #30 AWG (2 strands) Bifilar Wound

Core: Ferro cube EC35-3C8

Bobbin: Ferro cube EC35PCB1

Gap $\approx 0.01$ " for a primary inductance of 1.0 mH

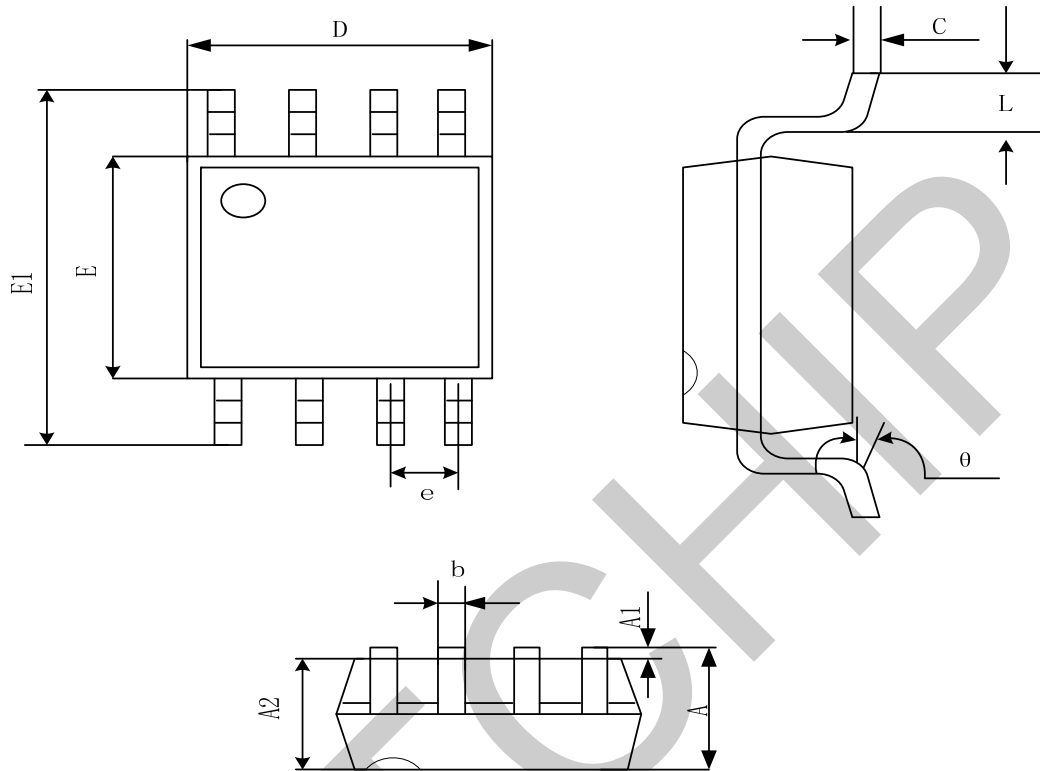
Test	Conditions	Results
Line Regulation: 5.0 V ±12 V	Vin=95 to 130 Vac	$\Delta = 50 \text{ mV}$ or $\pm 0.5\%$ $\Delta = 24 \text{ mV}$ or $\pm 0.1\%$
Load Regulation: 5.0V ±12V	Vin=115 Vac, Iout= 1.0 A to 4.0 A Vin=115 Vac, Iout=100 mA to 300 mA	$\Delta = 300 \text{ mV}$ or $\pm 3.0\%$ $\Delta = 60 \text{ mV}$ or $\pm 0.25\%$
Output Ripple: 5.0 V ±12V	Vin=115 Vac	40 mVp.p 80 mVp-p
Efficiency	Vin=115 Vac	70%

All outputs are at nominal load currents unless otherwise noted.

Pin Function Description		
Pin No.	Function	Description
1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	RT/CT	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground. Operation to 500 kHz is possible.
5	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).
6	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	VCC	This pin is the positive supply of the control IC.
8	Vref	This is the reference output. It provides charging current for capacitor CT through resistor RT.

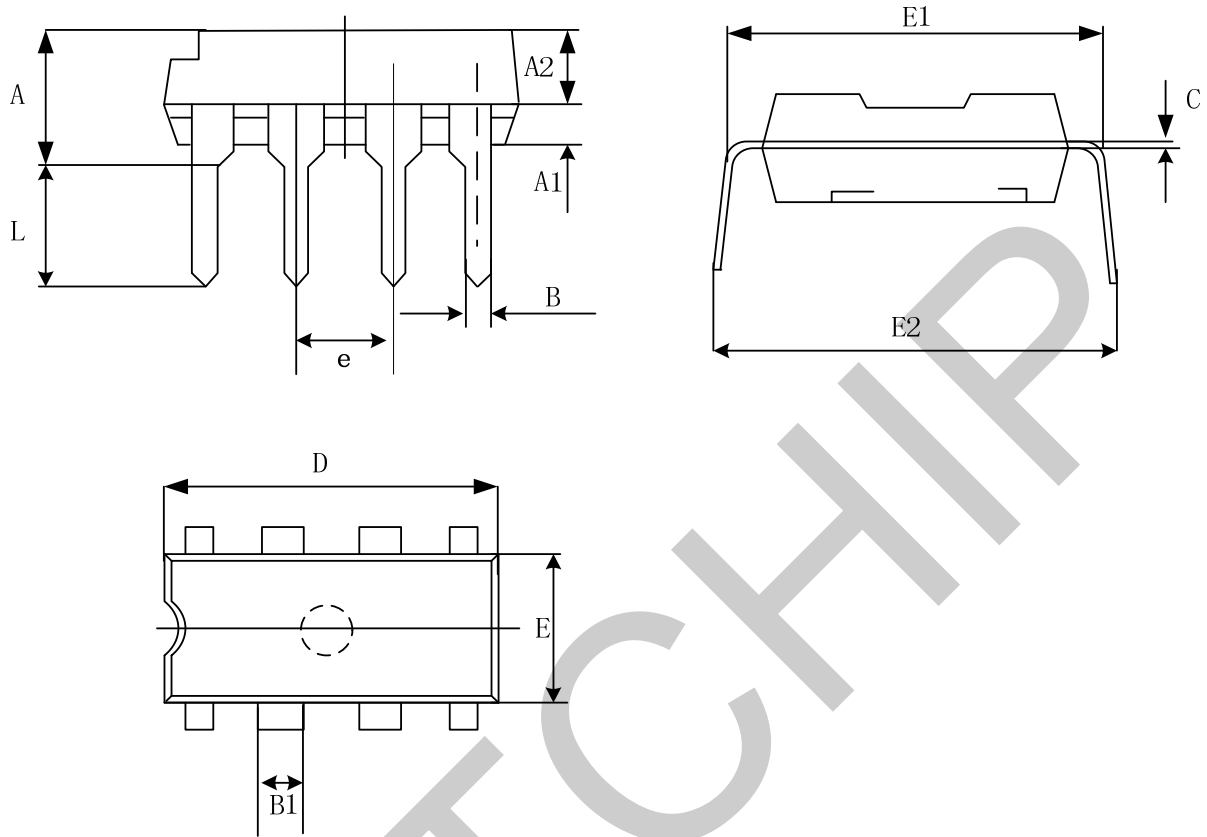
### PACKAGE MECHANICAL DATA

SOP- 8



Symbol	Dimensions In Millimeters(mm)	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
C	0.170	0.250
D	4.700	5.100
E	3.800	4.00
E1	5.800	6.2
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

DIP-8



Symbol	Dimensions In Millimeters(mm)	
	Min	Max
A	3.710	4.310
A1	0.500	
A2	3.200	3.600
B	0.350	0.620
B1	1.524(BSC)	
C	0.204	0.360
D	9.000	9.500
E	6.200	6.600
E1	7.320	7.920
e	2.540(BSC)	
L	3.000	3.600
E2	8.200	9.000